REMARKS

Claims 1-7 and 10-12 remain in this application. Claims 8 and 9 have been canceled without disclaimer. Claims 1 and 7 have been amended. New claim 12 has been added. Claims 1 and 7 were amended to better recite the invention. New claim 12 has been added to recite: "means for applying a steady negative back bias to a NMOS region of said substrate and for increasing" and "wherein said means is a negative voltage source." No new matter has been added.

Interview Summary by Inventors

Inventors, Dr. Summers and Eric Jackson, and applicants' attorney, Jane Barrow, had an interview on July 17, 2003, with Examiner Nguyen and Supervisory Patent Examiner Eddie Lee. Applicants and Jane Barrow wish to thank the Examiner Nguyen and Supervisory Patent Examiner Eddie Lee for the interview. The Interview Summary reflects the discussion. Applicants are to respond to the Office Action of February 25, 2003, indicate the existence of unexpected results as shown in FIG 3 of the patent application, discuss the lack of motivation to combine the references, discuss that the combination of Park et al. and Terrill et al. would not give the structure of the recited in the claims and that the claims specifically state that the present invention relates to "bulk CMOS or NMOS" and that this means and is stated in the claims that there is no oxide layer beneath the FETs. In addition, it was noted in the interview that there is an inadvertent error on page 2 of the February 25, 2003, office action with regard to Terrill et al.'s disclosure.

Requirement for Prima Facie Obviousness

Claims 1-11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Park et al. in view of Terrill et al.

A prima facie case of obviousness is established when the Examiner provides:

a. References;

b. References that teach;

c. References that are available to the inventors

d. A suggestion to combine/modify the references; and

e. Evidence that the combination/modification would have made the claimed invention obvious to one of ordinary skill in the art. In re Wilder, 166 U.S.P.Q. 545, 548 (C.C.P.A. 1970); In re Rinehart, 189 U.S.P.Q. 143, 147 (C.C.P.A. 1976); In re Fine, 5 U.S.P.Q.2D 1596, 1598 (Fed. Cir. 1988); and In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992).

If any one of these elements is not established, then the Examiner's option of obviousness is deficient and Applicants are deserving of a patent with respect to this issue, In re Oetiker, 24 U.S.P.Q.2D 1780, 1783 (Fed. Cir. 1992).

1. References:

The Examiner has cited two references, Park et al. and Terrill et al.

2. References that teach:

The second element requires that the references place the invention in the public domain prior to the date of invention, i.e., the references combine to render the claimed subject matter obvious.

The present invention as recited in claim 1 relates to a bulk CMOS or NMOS device that is resistant to total dose radiation failures due to charge build up in a field oxide. The elements of the device are:

a Si substrate:

one or more FETS on the substrate;

a field oxide region separating each FET; and

a negative voltage source for applying a steady negative back bias to a NMOS region of the substrate and for increasing the threshold voltage of the field oxide region to reduce leakage currents due to radiation damage in said field oxide region thereby mitigating total dose radiation effects; and

wherein a bulk CMOS or NMOS device does not include an insulator layer beneath said FETs.

Claim 1 as previously presented reiterated that bulk CMOS or NMOS (not a SOI) means that there is no insulator layer beneath the FETs.

Applicants' Claimed Invention

In sum, applicants' claims bulk CMOS or NMOS further includes a negative voltage source, i.e., the transistor will have at least four wires, source, drain,

gate and negative voltage source. The negative voltage source is for applying a steady negative back bias to a NMOS region of said substrate and for increasing the threshold voltage of the field oxide region to reduce leakage currents due to radiation damage in the field oxide region thereby mitigating total dose radiation effects.

Park et al.'s Disclosure

Park et al. in Fig. 4 (prior art) discloses a bulk CMOS device as it contains a source, a drain, a gate, a field oxide region and a Si substrate. Park et al. does not contain an insulator layer beneath the FETs. Park et al. does not disclose a negative voltage source for applying a steady negative back bias to a NMOS region of said substrate and for increasing the threshold voltage of the field oxide region to reduce leakage currents due to radiation damage in the field oxide region thereby mitigating total dose radiation effects.

Terrill et al.'s Disclosure

Terrill et al. relates to an SOI. Terrill et al. contains a source, a drain, a gate, an insulator layer beneath the FETs, a back-gate bias producing an electric field which induces charged carriers in the channel region without having to introduce dopants into the channels (Co. 3, lines 37-40) and a Si substrate. Again, as Terrill et al. relates to an SOI, there is a buried insulator layer 4. Terrill et al. does not disclose a negative voltage source for applying a steady negative back bias to a NMOS region of said substrate and for increasing the threshold voltage of the field oxide region to reduce leakage currents due to radiation damage in the field oxide region thereby mitigating total dose radiation effects.

3. References that are available to the inventors:

The third element specifies that the references relied upon as prior art be in the inventors' endeavor, or reasonably pertinent to the specific problems in which the inventors were involved, i.e., analogous prior art. In re Antle, 170 U.S.P.Q. 285, 287-288 (C.C.P.A. 1971).

The Federal Circuit has stated in In re Clay, 23 U.S.P.Q.2D 1058, 1060-61 (Fed. Cir. 1992), that:

> [A] reference is reasonably pertinent if ... it is one which, because of the matter with which it deals, logically would have commended itself to the

inventor's attention in considering his problem... If a reference disclosure has the same purpose as the claimed invention, the reference relates to the same problem ... if it is directed to a different purpose, the inventor would accordingly have had less motivation or occasion to consider it.

The Problem To Be Solved by Park et al. and Terrill et al.

Neither Park et al. nor Terrill et al. are analogous prior art, as they do not state the same purpose or try to solve the same problem as that of the present invention. The Park et al. solves a problem of CMOS integrated circuits and fabrication methods that can reduce the likelihood of overlap between regions thereof, notwithstanding decreasing device dimensions. Terrill et al. solves a SOI problem by applying a back–gate bias voltage to a SOI CMOS to avoid punchthrough and other short-channel effects. Terrill et al. does not disclose the problem of radiation in the CMOS device. In Terrill et al. it is stated that: "applied back-gate bias produces an electric field with induces charged carriers in the channel region" Col. 3, lines 37-39.

Purpose of Applicants' Claimed Invention

The purpose of Applicant's device is to overcome the accumulation of radiation dose from a radiation environment, e.g., space, altitudes of at least 20,000 feet above sea level, industrial, medical or military environments where there is sufficiently high average fluxes of ionizing radiation, delivering a dose on the order of tens or hundreds of krad over the period of use of the CMOS device. This total dose radiation failure arises in the field oxide region of the device. It is thought that this negative bias raises the threshold voltage in the field oxide region. The larger negative bias will make the device harder against total dose radiation, something that researchers are spending millions of dollars trying to do. See, page 7, lines 9-14 and Page 5, lines 13-14.

Thus, both of these references should be removed as prior art to the determination of a prima facie case of obviousness because neither Park et al. nor Terrill et al. is reasonably pertinent or analogous art. Thus, the Examiner has not established the third element of a prima facie case of obviousness, and Applicants should be provided with a patent.

3. A suggestion to combine/modify the references:

The fourth element requires some reason, suggestion or motivation from the prior art as a whole that indicates that the person of ordinary skill would have combined or modified the references. The Board of Patent Appeals and Interferences has stated in Ex parte Skinner, 2 U.S.P.Q.2d 1788, 1790 (BPAI 1987): "When the incentive to combine the teachings of the references is not readily apparent, it is the duty of the examiner to explain why combination of the reference teachings is proper ... Absent such reasons or incentives, the teaching of the references are not combinable." In re Fritch, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992), teaches that an Examiner cannot simply cite different features of the claimed invention from different sources unless the Examiner explains the suggestion or motivation to combine or modify the prior art references.

The February 25, 2003, Office Action

The examiner has mistakenly stated in his office action of February 25, 2003, that:

> Regarding claim1. Park et al. discloses on figure 4 a bulk CMOS device **A. [resistant to total dose radiation failures due to charge build up in a field oxide],** the device comprising a Si substrate 2; two or more FETs on said substrate; a field oxide region 4 separating each FET; and wherein a bulk CMOS device does not include an insulator layer beneath said FETs. Park et al. does not disclose a negative voltage source for applying a steady back bias to a NMOS region of said substrate to increase the threshold voltage of the field oxide region thereby mitigating total dose radiation effects. However, Terrill et al. discloses on figure 2 a negative voltage source **B. [for applying a steady back bias to a NMOS region of said substrate to increase the threshold voltage of the field oxide region thereby mitigating total dose radiation effects.] C. [In view of such teachings, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Park et al. by having a negative voltage source for applying a steady back bias to NMOS region of said substrate to increase the threshold voltage of the field oxide region to reduce leakage currents due to radiation damage**

in said field oxide region thereby mitigating total dose radiation effects for the purpose of obtaining excellent turn off sub threshold and Transconductance characteristics as taught by Terrill et., Col 1, lines 65-66.]

In brackets A, B and C is contained misstated understanding of Park et al. and Terrill et al. by the Examiner.

A. In the **A. bracketed recitation**, the examiner misstates Park et al., as Park et al. is not concerned with total dose radiation or any kind of radiation. The purpose of Park et al. relates to CMOS integrated circuits and fabrication methods, which can reduce the likelihood of overlap between regions thereof, notwithstanding decreasing device dimensions, Col. 1, lines 20-32.

B. In the **B. bracketed recitation,** the examiner misstates Terrill et al. as Terrill et al. does not apply a steady back bias to NMOS region of said substrate to increase the threshold voltage of the field oxide region... Terrill et al. discloses applying a back–gate bias voltage to a SOI CMOS to avoid punchthrough and other short-channel effects, Col. 3, lines 31-33.

C. In the **C. bracketed recitation,** the examiner concludes that in view of such teachings, it would be obvious .... No, obviousness has not been established and clearly cannot be established here. There must be a motivation or suggestion to combine the references. The Examiner has no provided or motivation or suggestion to combine the cited references.

A disclosure in a figure is not a "teaching." The Federal Circuit stated in In re Fritch, 23 U.S.P.Q.2d 1780, 1783-84 (Fed. Cir. 1992) that:

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. Under Section 103, teachings or references can be combined only if there is some suggestion or incentive to do so. (quoting ACS Hosp. Systems, Inv. v. Montefiore Hosp., 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984) ... The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the invention.

The Board of Patent Appeals and Interferences in In re Regel, Buchel and Plemp"el, 188 U.S.P.Q. 136, 139 (BPAI 1975) stated in footnote 6:

> As we have stated in the past, there must be some logical reason apparent from positive, concrete evidence of record which justifies a combination of primary and secondary references." In re Stemniski, supra. Further as we stated in In re Bergel, 130 U.S.P.Q.2d (C.C.P.A. 1961): "The mere fact that it is possible to find two isolated disclosures which might be combined in such a way to produce a new compound does not necessarily render such production obvious unless the art also contains something to suggest the desirability of the proposed combination." Applicants have provided a few quotes from the case law for the Examiner.

The examiner has not directed applicants' attention to a teaching or suggestion within either Park et al. or Terrill et al. to combine them. "It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that "one cannot use hindsight construction to pick an choose among isolated disclosures in the prior art to duplicate the claimed invention." In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

The Examiner has taken a prior art teaching from Park et al., Fig. 4, and then the Examiner took an element from Terrill et al. using the disclosure of the present invention without any suggestion or teaching in either cited reference and stated applicants' invention is obvious. It is impermissible to use applicants' disclosure in this manner, in addition, it is impermissible not to have the requisite suggestion or teaching to combine the cited references. This is a difficult concept to understand.

One example of a defective obviousness rejection is a rejection, which includes separate references to represent each of the different features described in the applicants' claims. In this situation, the Examiner uses the claims as the guide in attempting to piece together the claimed invention. The principal objection to the Examiner formulating the rejection in this manner is that the Examiner does not provide any suggestion or motivation to combine the various prior art references together. Thus, the Examiner has, in effect, used the claims of the patent as an instruction manual to find the appropriate prior art, which might render the claims obvious. In this situation, the Examiner has lost

sight of the real issue: whether it would have been obvious to combine the references without having access to the application under examination to arrive at the claimed invention as a "whole." The Federal Circuit stated recently in Chemical Separation Technology Inc. v. US, 63 U.S.P.Q.2d 1114, 1155 (Fed. Cir. 2002), that:

> To be sure, one skilled in the art, closeted in her office, with all the cited prior art conveniently selected and arrayed before her, might have compiled claims equivalent to those in the patent. But, if the case law stresses anything in regards to combination, it is that obviousness is not to be implied simply because all the pieces to a puzzle are present somewhere. Rather, like a real jigsaw puzzle, there must be some suggestion in the art of a complementing association, some teaching providing a guiding framework, or at very least, some **notching** or padding of the puzzle pieces themselves, that would lead or incentivize one skilled in the art to derive the combination that is, in the end result, the claim.

Thus, the Examiner has not established the fourth requirement of a prima facie case of obviousness and thus has not established a prima facie case of obviousness, and Applicants should be provided with a patent.

5. Evidence that the Examiner has not established the requirement of a prima facie case of obviousness, and the applicants should be provided with a patent.

The final element is that the resulting combination or modification appears to show or suggest the claimed invention. This determination involves assuming, for purposes of the analysis, that all of the teachings of the individual references in the cited combination are combined to form what is, essentially, a single reference. Then, the language in each rejected claim is compared with this combination "reference" in an element by element anticipation-style examination.

The Combination of Park et al. and Terrill et al.

Thus, if both Park et al. and Terrill et al. are combined, one would have an insulator beneath the FET as that is what Terrill et al. requires as Terrill et al. relates to a SOI. But, the claims specifically exclude an insulator beneath the FETs by stating "bulk" CMOS or NMOS and by restating what bulk means in the body of the claim, "wherein a bulk CMOS or NMOS device does not include an insulator layer beneath said FETs."

None of the cited references in combination suggest or teach the present invention as claimed in claims 1-7 and 9-12.

Unexpected Results in the Application

There is comparative data already found in the present application, see In re Margois, 785 F.2d 1029 (Fed. Cir. 1986). Applicants want to have it noted that FIGs 3-5 show unexpected results when a back bias is applied.

Fig. 3 shows a dose of 100 krad of radiation exposure bulk NMOS with $V_b = 0V$, and $V_b = -1.6, -2.0$ and -3.3 back bias applied. The transistors tested were produced by a commercial vendor as noted in Example 2. The only change to the standard processing procedure was the addition of the back bias connection. A back bias voltage of zero corresponds to the standard operating conditions of commercial CMOS. One can easily note that after irradiation of the device the source-drain current for gate voltages less than 0 V, when the transistor is supposed to be off, is increased by about 4 orders of magnitude. This is typical of unhardened CMOS. As the magnitude of the back bias voltage increases this leakage current is progressively reduced to a level below the unirradiated value. It is thought this occurs because charge accumulated in the field oxide inverts the Si under the oxide the same way a voltage applied to the gate of a transistor inverts the channel. Back bias affects this field oxide "transistor" in a manner similar to a normal transistor, but the effect is much larger.

The threshold voltage can be defined to be the voltage where the current is 0.1 nA. Then the measured threshold will be the lower of the threshold voltages of the transistor and the field oxide region. It can be seen that the threshold of the field oxide region is less than –2 V with 0 V back bias, and is greater than or equal to the threshold of the transistor with –3.3 V back bias. This demonstrates that the threshold voltage of the field oxide region increases with back bias much more rapidly than the threshold voltage of the transistor. See Example 2.

Figs. 4 and 5 also show the unexpected results when a back bias is applied. The difference from the previous example is primarily in the operating state of the transistor during irradiation. Application of a voltage to the gate during the irradiation is known to increase the unwanted charge accumulation in the field oxide. Fig. 5 shows that the back

biased NMOS can still be radiation tolerant when the back bias is applied during irradiation.

The Examiner has not established the fifth requirement of a prima facie case of obviousness, and Applicants should be provided with a patent.

As claims 2-6 depend from amended claim1 and contain all the limitations of claim 1, it is felt that claims 2-6 distinguish from the cited references in the same manner as amended claim 1. As claims 10-11 depend from amended claim 7 and contain all the limitations of claim7, it is felt that claims 10-11 distinguish from the cited references in the same manner as amended claim 12. See, Chemical Separation Technology Inc. v. US, 63 U.S.P.Q.2d 1114, 1138 (Fed. Cir. 2002)

The test of Section 103 is not whether an improvement or a use set forth in a patent would have been obvious or nonobvious; rather the test is whether the claimed invention, considered as a whole, would have been obvious. Jones v. Hardy, 220 U.S.P.Q. 1021, 1024 (Fed. Cir. 1984). The Federal Circuit in Jones stated:

> Though it is proper to note the differences in a claimed invention from the prior art, because the difference may serve as one element in determining the obviousness/nonobviousness issue, it is improper (even if erroneously suggested by a party) to consider the difference as the invention. The "difference" may have seemed slight (as has often been the case with some of history's great inventions, e.g., the telephone), but it may also have been the key to success and advancement in the art resulting from the invention. Further, it is irrelevant in determining obviousness that all or all other aspects of the claim may have been well known in the art. Hence the statute, the law established not by judges but by Congress, requires that the invention as claimed be considered "as a whole" when considering whether the invention would have been obvious when it was made. Id. at 1024.

Thus, it is impermissible to focus on the "gist" or "core" of the invention, Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc., 230 U.S.P.Q. 416, 420 (Fed .Cir. 1986), or on specific differences between the claimed invention and prior art, Jones at 220 U.S.P.Q. at 1024. Moreover, the invention as a whole is not restricted to the specific

subject matter claimed, but also embraces its properties of that structure and the problems which it solves. In re Wright, 6 U.S.P.Q.2d 1959, 1961 (Fed. Cir. 1988).

Similarly, the references must be taken in their entireties, including those portions which argue against obviousness. Bausch & Lomb, 230 U.S.P.Q. at 420. "It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to a full appreciation of what such reference fairly suggests to one skilled in the art." Id. at 419. The courts have long cautioned that consideration must be given "where the references diverge and teach away from the claimed invention." Akzo N.V. v. International Trade Commission, 1U.S.P.Q.2d 1241, 1246 (Fed. Cir. 1986).

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In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly the examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Respectfully submitted,

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